1   METHOD AND APPARATUS FOR NONCOHERENT SIGNAL PROCESSING IN

2   PILOTLESS WIRELESS SYSTEMS

3

4   BACKGROUND OF THE INVENTION

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6   1. Field of the Invention

7   The present invention relates to telecommunications. The invention more

8   particularly relates to wireless telecommunications apparatus, systems and methods

9   which implement data transmission via a plurality of telecommunication channels such as

10   radio channels with variable parameters, including multipath wireless channels. More

11   specifically, the invention relates to pilotless wireless systems with mobile transmitters

12   and/or receivers, although it is not limited thereto.

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14

15   2. State of the Art

16   Development of pilotless data transmission and signal processing is an important

17   problem of wireless system design. Pilotless wireless systems provide the highest real

18   data rate by utilizing system capacity exclusively for data transmission and providing all

19   receiving functions without any accompanying pilot signals.

20

21   One manner of implementing a pilotless system is using coherent demodulation

22   based on a reference signal and extracting all necessary information from signals-bearing

23   data. In this case, precise estimation and tracking of the carrier phase plays a critical role.

24   A conventional approach to carrier phase estimation is described in John Proakis, "Digital

25   Communications", McGraw Hill, Fourth Edition, 2000, Sections 6.2.4 -6.2.5 which is

26   hereby incorporated herein in its entirety.   A new method of carrier phase tracking was

1   proposed in co-owned U.S. Serial No. 10/628,943 filed July 29, 2003, and entitled

2   "Pilotless, Wireless, Telecommunications Apparatus, Systems and Methods" which is

3   also hereby incorporated by reference herein in its entirety. In that invention, phase

4   tracking is based on reducing and averaging differential quadrature components of

5   received symbols.

6

7   Coherent processing, based on carrier phase tracking, provides the maximum

8   possible performance in channels with comparatively slow phase changing and

9   comparatively high signal-to-noise ratio (SNR). If one of those conditions is not

10   satisfied, the coherent demodulator loses its advantages. For example, when the bit error

11   rate BER> 0.01, phase estimation becomes less precise. The SNR penalty depends on the

12   method of phase tracking but it may reach 1-2 dB. However, much more performance

13   loss can be caused by fast phase changing or, especially, phase jumping. Fast phase

14   changing and phase jumping are typical phenomenon in communications involving

15   mobile clients because in the mobile environment the multipath configuration may

16   change instantly. This change can cause coherent detection degradation even at a

17   comparatively high SNR because any phase tracking algorithm, based on symbol

18   averaging, is not capable of instantly estimating the phase changing. As a result, the

19   coherent receiver provides a long sequence (burst) of errors after phase jumping even at a

20   comparatively high SNR. This is the reason why wireless system designers consider

21   approaches other than coherent processing for pilotless systems.

22

23   For multipath radio channels in a mobile environment, a promising manner of

24   implementing a pilotless system involves the utilization of noncoherent signal processing

25   which does not need any information about the initial phase of the reference signal and

26   consequently does not require phase tracking at all. In the case of phase modulation,

1 noncoherent processing can be only used in combination with Differential Phase Shift

2 Keying (DPSK) in contrast to coherent processing which can be used with both DPSK

3 and PSK. As is emphasized in Dariush Divsalar, and Marvin Simon, "Multiple-Symbol

4 Differential Detection of MPSK", IEEE Transactions on Communications, vol.38, N3,

5 March 1990 (which is hereby incorporated by reference in its entirety), for multipath

6 channels with fast phase changing, a DPSK-with-noncoherent-processing scheme is the

7 only way to provide robust data transmission.

8

9   Conventional noncoherent DPSK processing includes a two-symbol interval for

10 making a decision. With a two-symbol interval, if a phase jump occurs during the

11 symbol interval, only one error will take place. However, two-symbol non-coherent

12 DPSK suffers from a performance penalty when compared to ideal coherent DPSK. For

13 example, at BER=10^{-5} the penalty is about 0.75 dB for DBPSK (Differential Binary

14 PSK), and about 2.2 dB for DQPSK (Differential Quadrature PSK). For M-ary DPSK

15 (DMPSK) the penalty increases with increasing M.

16

17   A well-known way to mitigate the performance loss of the non-coherent receiver

18 and preserving its advantages is to increase the interval of the non-coherent processing.

19 This approach, known as multisymbol non-coherent detection (or processing) was

20 considered in the previously incorporated article by Dariush Divsalar, and Marvin Simon.

21 The conventional approach to multisymbol processing is based on allowing the

22 observation interval over which symbol decisions are made to be more than a two-symbol

23 interval while at the same time making a joint decision on several symbols

24 simultaneously as opposed to symbol-by-symbol decisions. An obvious disadvantage of

25 the joint decision on several symbols is the additional symbol delay which results in the

1 receiver. In addition, the joint decision procedure is undesirable for some decoding

2 algorithms.

3

4 <center>SUMMARY OF THE INVENTION</center>

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6 It is therefore an object of the invention to provide pilotless telecommunication

7 systems and associated methods and apparatus, which transmit data by means of DPSK

8 modulation of carriers and which provide all receiving functions based on multisymbol

9 noncoherent processing of carriers.

10

11 It is another object of the invention to provide general methods and apparatus for

12 multisymbol noncoherent processing in single-carrier and multi-carrier systems with

13 symbol-by-symbol decisions.

14

15 It is a further object of the invention to provide relatively simply implementable

16 algorithms for multisymbol noncoherent processing of M-ary DPSK modulated signals.

17

18 It is an additional object of the invention to provide simple iterative algorithms of

19 multisymbol noncoherent processing of DPSK modulated signals, when each next

20 symbol may be simply combined with a result of previous symbol processing(s).

21

22 Another object of the invention is to provide pilotless wireless telecommunication

23 systems, apparatus, and methods which provide all receiving functions without pilot

24 signals by means of multisymbol noncoherent processing with symbol-by-symbol

25 decisions which are based on iterative algorithms.

26

1   In accord with the above objects which will be discussed in more detail below, the

2   present invention provides methods, and apparatus for the realization of pilotless

3   telecommunication systems, which use the entire system capacity exclusively for data

4   transmission, and which provide all receiving functions based on an iterative multisymbol

5   noncoherent processing of carriers with symbol-by-symbol decision-making.

6

7   According to the invention, a method or algorithm is provided for 3-symbol

8   noncoherent processing of M-ary DPSK (DMPSK) modulation with an arbitrary set of

9   phase differences. The preferred algorithm is a three-step procedure. The first two steps

10   are iterative, with the first step being the calculation of two-symbol quadrature

11   components, and the second step being the calculation of three-symbol quadrature

12   components of final three-symbol vectors. The lengths of the vectors are then compared

13   in the third step to find the maximum. The algorithm is preferably implemented with a 3-

14   symbol DPSK-signal noncoherent demodulator which utilizes intersymbol processors,

15   memory registers and a decision block.

16

17   The preferred algorithm of the invention has a desirable iterative structure in that

18   the 3-symbol quadrature components are sums of the previous 2-symbol components and

19   transformed quadrature components of the current symbol. The preferred algorithm of

20   the invention provides the ability to make a symbol-by-symbol decision and/or a joint

21   decision on two symbols simultaneously.

22

23   According to another aspect of the invention, a simplified algorithm for 3-symbol

24   noncoherent processing of DQPSK signals is provided.

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1　　　　According to a further aspect of the invention, a general algorithm for N-symbol

2　　noncoherent processing of M-ary DPSK signals is provided. The general algorithm is

3　　carried out with (N-1) recurrent steps (iterations) plus a decision step. Each iterative step

4　　includes a simple trigonometrical transformation of quadrature components of the current

5　　symbol and a sum of the transforms with the results of the previous step. A final N-

6　　symbol based decision regarding the current transmitted symbol corresponds to the vector

7　　of maximum length, calculated after the (N-1)-th step of the recurrent procedure. The

8　　general algorithm is optionally implemented with (N-1) intersymbol processors, (N-2)

9　　pairs of memory blocks for saving results of the intersymbol processors, a decision block,

10　　and two shift registers for quadrature components of the received signal. Alternatively, a

11　　single processor may be used for all functions of the intersymbol processors, and one or

12　　more memory blocks may used to implement the memory blocks and shift registers.

13

14　　　　Additional objects and advantages of the invention will become apparent to those

15　　skilled in the art upon reference to the detailed description taken in conjunction with the

16　　provided figures.

17

1   BRIEF DESCRIPTION OF THE DRAWINGS

2

3   Figure 1 is a high level block diagram of a single carrier receiver incorporating a

4   multisymbol noncoherent demodulator according to the invention.

5

6   Figure 2 is a high level block diagram of a multicarrier receiver incorporating a

7   multisymbol noncoherent demodulator according to the invention.

8

9   Figure 3 is a schematic diagram of a 3-symbol noncoherent demodulator of DPSK

10   signals according to the invention.

11

12   Figure 4 is a schematic diagram of the intersymbol processor and memory

13   registers of the 3-symbol noncoherent demodulator of Fig. 3.

14

15   Figure 5 is a schematic diagram of the decision block of the 3-symbol

16   noncoherent demodulator of Fig. 3.

17

18   Figure 6 is a schematic diagram of an N-symbol noncoherent demodulator of

19   DPSK signals according to a second embodiment of the invention.

20

21   Figure 7 is a high level schematic diagram of an alternative second embodiment

22   of the invention which utilizes a high speed intersymbol processor in an N-symbol

23   noncoherent demodulator of DPSK signals.

24

25   Figure 8 is a graph showing results of a stochastic simulation of the algorithms of

26   the invention, with the bit error rate (BER) plotted as a function of signal-to-noise ratio

1   (SNR) for DBPSK modulation and noncoherent processing with 2, 3, 4, and 5-symbol

2   intervals.

3

4   Figure 9 is a graph showing results of a stochastic simulation of the algorithms of

5   the invention, with the bit error rate (BER) plotted as a function of signal-to-noise ratio

6   (SNR) for DQPSK modulation and noncoherent processing with 2, 3, 4, and 5-symbol

7   intervals.

8

9

10   DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

11

12   Turning now to Fig. 1, a block diagram of a single carrier receiver 10 is shown.

13   Receiver 10 includes a channel interface 12, an in-phase/quadrature (I/Q) detector 14, a

14   multisymbol noncoherent demodulator of the invention 20, and a decoder 22. In the case

15   of a wireless system, the channel interface 12 typically includes an antenna, a low noise

16   amplifier, and possibly a signal transformer which transforms the signal to an intermediate

17   frequency. The I/Q detector 14 typically includes two multipliers 23a, 23b, two low pass

18   filters 24a, 24b, a local oscillator 25, and a phase rotator 26. As is well known in the art,

19   the I/Q detector takes the signal (possibly, the intermediate frequency signal) from the

20   channel interface and provides quadrature components X, Y to the demodulator 20.

21   Determinations of the demodulator 20 are provided to the decoder 22. According to the

22   invention, different implementations of channel interfaces, I/Q detectors and decoders

23   may be utilized as are known in the art.

24

25   A block diagram of an OFDM (orthogonal frequency division multiplexed)

26   multicarrier receiver 10' is shown in Fig. 2. Receiver 10' includes a channel interface 12,

1   an I/Q detector 14, a fast Fourier transformer (FFT) 15, a multisymbol noncoherent

2   demodulator of the invention 20', and a decoder 22'. The channel interface 12 preferably

3   includes the same elements as in the single carrier system of Fig. 1. The FFT 15 provides

4   quadrature components of all carriers for the received signal. The output of the FFT is a

5   set of quadrature components X_{cn} and Y_{cn} for carrier numbers (cn)=1,2,...L where L is the

6   number of carriers of the multicarrier system. The multisymbol noncoherent demodulator

7   20' processes each pair of quadrature components in parallel or in a consecutive manner

8   depending on desired implementation. The output of the demodulator 20' is provided to

9   decoder 22'. Again it will be appreciated that different implementations of channel

10   interfaces, I/Q detectors, Fourier transformers (or equivalents), and decoders may be used

11   as are known in the art.

12

13   Prior to turning to the figures showing the noncoherent demodulators of the

14   invention, a discussion of the theoretical underpinnings of the demodulators of the

15   invention is useful. First, it is desirable to consider 2-symbol and 3-symbol noncoherent

16   processing of M-ary DPSK (DMPSK) modulation with a set of phase differences

17         $\Delta(k)$; $k = 1, 2, ..., M.$ (1)

18

19   In particular, define $X(q)$ and $Y(q)$ as the quadrature components (real and imaginary

20   parts) of the received signal at the q-th symbol interval, where q=1, 2, 3, ... It should be

21   noted that quadrature components $X(q)$ and $Y(q)$ are results of the convolution of the

22   received signal and the reference signal, or results of a Discrete Fourier Transform (DFT)

23   of the received signal based on a certain reference signal. For purposes of this discussion

24   it is assumed that the frequency of the reference signal is equal or "close enough" to the

25   frequency of the received signal. This means that the system preferably provides some

26   sort of frequency offset compensation, which is one of the conventional receiver

1 functions. Frequency offset compensation allows a receiver to mitigate SNR degradation

2 in the case of single carrier systems and avoid intercarrier interferences in the case of

3 multicarrier OFDM systems.

4

5 With these circumstances, the decision-making procedure for conventional 2-

6 symbol processing comprises two operations. The first operation is the calculation of the

7 2-symbol quadrature components VX_2 and VY_2 for all versions of the transmitted phase

8 differences $\Delta(k)$ according to:

9

10 $\qquad VX_2(k_1) = X(q-1) + X(q)\cos[\Delta(k_1)] + Y(q)\sin[\Delta(k_1)],$ $\qquad$ (2a)

11 $\qquad VY_2(k_1) = Y(q-1) + Y(q)\cos[\Delta(k_1)] - X(q)\sin[\Delta(k_1)],$ $\qquad$ (2b)

12 where $q=2, 3, \ldots$; and $k_1=1, 2, \ldots, M$.

13

14 In equations (2a) and (2b), the consequent (current) symbol is reduced to the most likely

15 preceding symbols. It is possible to use the inverse transformation: reduction of the

16 preceding symbol into the most likely consequent symbols. Which option is utilized

17 depends on the direction of the phase difference reading, but the final result of the

18 decision making will be the same. In the following, reduction of the consequent symbol

19 into the possible preceding symbols is utilized.

20

21 The second operation for conventional 2-symbol processing is finding the index

22 "k_1" corresponding to the maximum vector length:

23

24 $\qquad \max\{\ [VX_2(k_1)]^2 + [VY_2(k_1)]^2\};\ k_1=1, 2, \ldots, M.$ $\qquad$ (3)

25

It is noted that M sets of quadrature values are calculated in the first operation, and the M values in the square brackets of (3) are compared to find the maximum.

According to the invention, a symbol-by-symbol decision-making algorithm for a 3-symbol processing interval starts with the determination of the quadrature components VX_2 and VY_2. These components in the 3-symbol case, for the q-th, (q-1)-th and (q-2)-th symbols are equal to

$$VX_2(k_1) = X(q-2) + X(q-1)\cos[\Delta(k_1)] + Y(q-1)\sin[\Delta(k_1)], \qquad (4a)$$

$$VY_2(k_1) = Y(q-2) + Y(q-1)\cos[\Delta(k_1)] - X(q-1)\sin[\Delta(k_1)]. \qquad (4b)$$

Variables UX_3 and UY_3 can now be defined corresponding to the transformation of the quadrature components $X(q)$ and $Y(q)$ of the current q-th symbol for each possible combination of phase differences $\Delta(k_1)$ between the (q-2)-th and (q-1)-th symbols, and $\Delta(k_2)$ between the (q-1)-th and q-th symbols according to:

$$UX_3(k_1,k_2) = X(q)\cos[\Delta(k_1)+ \Delta(k_2)] + Y(q)\sin[\Delta(k_1) + \Delta(k_2)] \qquad (5a)$$

$$UY_3(k_1,k_2) = Y(q)\cos[\Delta(k_1) + \Delta(k_2)] - X(q)\sin[\Delta(k_1) + \Delta(k_2)]. \qquad (5b)$$

Now, to find the 3-symbol quadrature components VX_3 and VY_3, transforms (5) are added to the previously calculated values (4):

$$VX_3(k_1, k_2) = VX_2(k_1) + UX_3(k_1, k_2); \qquad (6a)$$

$$VY_3(k_1, k_2) = VY_2(k_1) + UY_3(k_1, k_2). \qquad (6b)$$

1   Finally, a decision is made by finding a maximum:

2

3   Max $\{ [VX_3(k_1, k_2)]^2 + [VY_3(k_1, k_2)]^2 \}$,   (6c)

4   where $k_1 = 1, 2, ..., M$, and $k_2 = 1, 2, ..., M$.

5

6   So, the algorithm for 3-symbol processing interval can be described as a three step

7   procedure: the first step is calculating 2-symbol quadrature components VX_2 and VY_2

8   according to equations (4a) and (4b), and the second step is calculating 3-symbol

9   quadrature components VX_3 and VY_3 according to equations (6a) and (6b). The third

10   step is making a decision by finding the maximum value according to equation (6c).

11

12   According to equations (6a) and (6b), M components of VX_3 and M components

13   of VY_3 are calculated for each component VX_2 and VY_2, i.e., M^2 of pairs (VX_3, VY_3) can

14   be determined. According to the invention, the M^2 pairs of vector lengths are then

15   compared to find the maximum according to equation (6c). For example, in the case of

16   DQPSK (as discussed below), sixteen pairs of (VX_3, VY_3) are calculated and compared.

17

18   Two additional notes should be made regarding equations (6a) – (6c). First,

19   equations (6a) and (6b) have a desirable iterative structure in that the 3-symbol

20   quadrature components VX_3, VY_3 are the sums of the previous 2-symbol components

21   VX_2, VY_2 and the transformed quadrature components of the current symbol. Second,

22   the decision algorithm (6c) may be used for both a symbol-by-symbol decision and/or a

23   joint decision on two symbols simultaneously. In the case of a symbol-by-symbol

24   decision, maximization in (6c) is provided through indexes k_2, corresponding to phase

25   differences between the (q-1)-th and q-th symbols. In the case of the joint symbol

1 decision, maximization in (6c) is provided through the whole set of indexes k_1 and k_2,

2 corresponding to two sets of phase differences: i.e., the phase difference between the

3 (q-2)-th and the (q-1)-th symbols, and the phase difference between the (q-1)-th and the

4 q-th symbols.

5

6   To reiterate, according to the invention, an algorithm for a 3-symbol noncoherent

7 processing of DMPSK telecommunications signals can be described as follows:

8   a) Three consecutive symbols with indexes q, (q-1) and (q-2) are used to participate

9   in making a decision relative to the current (q-th) symbol, and the corresponding

10   quadrature components of those signals X(q) and Y(q), X(q-1) and Y(q-1), X(q-2)

11   and Y(q-2) are saved;

12   b) Quadrature components X(q-1),Y(q-1) and X(q-2),Y(q-2) are transformed into a

13   set of 2-symbol quadrature components VX_2 and VY_2 according to equations (4a)

14   and (4b) using each possible phase difference $\Delta(k_1)$, where $k_1 = 1, 2, \ldots, M$;

15   c) Quadrature components X(q) and Y(q) of the current symbol are transformed into

16   a set of transforms $UX_3(k_1, k_2)$ and $UY_3(k_1, k_2)$ according to equations (5a) and

17   (5b) for each possible combination of phase differences $\Delta(k_1)$ and $\Delta(k_2)$, where

18        $k_1 = 1, 2, \ldots, M$ and $k_2 = 1, 2, \ldots, M$;

19   d) Sets of 3-symbol quadrature components $VX_3(k_1, k_2)$ and $VY_3(k_1, k_2)$ are

20   combined by adding the results of b) and c) according to equations (6a) and (6b);

21   e) A final decision relative to the current (q-th) symbol is the phase difference of the

22   set of differences $\Delta(k_2)$, where $k_2 = 1, 2, \ldots, M$, corresponding to the maximum

23   length of vectors $[VX_3(k_1, k_2), VY_3(k_1, k_2)]$, according to equation (6c).

24

25   Fig. 3 shows a schematic diagram of the 3-symbol noncoherent demodulator of

26 DPSK signals 20a (corresponding to demodulator 20 of Fig. 1, or 20' of Fig. 2) according

1   to the invention, operating according to a) through e) above. In particular, the

2   demodulator 20a of the invention includes four identical delay elements D_1, D_2, D_3 and D_4

3   with delay times equal to symbol length T, two memories R_1 and R_2, two intersymbol

4   processors IP_1 and IP_2, and 3-symbol decision block Decision3.

5

6   The demodulator 20a operates as follows. Quadrature components X(q) and Y(q)

7   of the q-th received symbol are directly fed to intersymbol processor IP_2 and through

8   delay elements D_1-D_4. to intersymbol processors IP_1. In IP_1, two adjacent symbols

9   (X(q-1),Y(q-1)) and (X(q-2),Y(q-2)), preceding the current symbol (and found in the

10   delay elements D_1, D_2, D_3 and D_4), are processed according to equations (4a) and (4b) or

11   according to Table 1 (below) for DQPSK (as described hereinafter) to generate M pairs

12   of numbers VX_2 and VY_2 which are stored in memories R_1 and R_2, respectively. In the

13   case of DQPSK (as described below), the memories R_1 and R_2 store four numbers for

14   VX_2 and four numbers for VY_2. The numbers VX_2 and VY_2 from memories R_1 and R_2

15   together with current symbol (X(q),Y(q)) are fed to IP_2, where they are processed

16   according to equations (5a), (5b) and (6a), and (6b) (or according to Tables 5a and 5b for

17   DQPSK as described below). Intersymbol processor IP_2 generates numbers VX_3 and VY_3

18   which are fed to the decision block Decision3, where a decision is made according to

19   equation (6c). In the case of DQPSK, as described below, sixteen pairs of numbers

20   (VX_3, VY_3) participate in the decision making procedure.

21

22   According to one aspect of the invention, equations (6a) and (6b) may be

23   considerably simplified in certain circumstances. In particular, in DQPSK modulation

24   systems, a typical set of phase differences are:

25

26              $\Delta(k)= (0, \pi/2, \pi, 3\pi/2)$.   (7)

1   With that limited set of phase differences, values VX_2 and VY_2 calculated according to

2   equations (4a) and (4b) can be reduced as suggested in Table 1.

3

4   **Table 1:** Values VX_2 and VY_2 according to equations (4a) and (4b)

k_1	1	2	3	4
$\Delta(k_1)$	0	$\pi/2$	π	$3\pi/2$
VX_2	X(q-2)+ X(q-1)	X(q-2)+Y(q-1)	X(q-2)-X(q-1)	X(q-2)-Y(q-1)
VY_2	Y(q-2)+Y(q-1)	Y(q-2)- X(q-1)	Y(q-2)-Y(q-1)	Y(q-2)+ X(q-1)

5

6

7   From Table 1 it can be seen that the calculation of values VX_2 and VY_2 are reduced to

8   simple combinations (summation or subtraction) of quadrature components of the

9   adjacent received symbols.

10

11   Table 2 contains possible values of the sum $(\Delta(k_1)+ \Delta(k_2))$ modulo 2π found in the

12   square brackets of equations (5a) and (5b) for the DQPSK demodulator with phase

13   differences (7).

14

15   **Table 2:** All combinations of $[\Delta(k_1)+ \Delta(k_2)]$ modulo 2π for DQPSK.

k_1 \ k_2	1	2	3	4
1	0	$\pi/2$	π	$3\pi/2$
2	$\pi/2$	π	$3\pi/2$	0
3	π	$3\pi/2$	0	$\pi/2$
4	$3\pi/2$	0	$\pi/2$	π

16

1   Continuing with equations (5a) and (5b) for DQPSK, Tables 3a and 3b contain

2   sine and cosine functions of the combinations indicated in Table 2:

3

4   **Table 3a:** $\text{Sin}[\Delta(k_1) + \Delta(k_2)]$

5

k_1 \ k_2	1	2	3	4
1	0	1	0	-1
2	1	0	-1	0
3	0	-1	0	1
4	-1	0	1	0

6

7   **Table 3b:** $\text{Cos}[\Delta(k_1) + \Delta(k_2)]$

8

k_1 \ k_2	1	2	3	4
1	1	0	-1	0
2	0	-1	0	1
3	-1	0	1	0
4	0	1	0	-1

9

10

11   With the sine and cosine functions determined, Tables 4a and 4b contain values

12   for the transforms $UX_3(k_1, k_2)$ and $UY_3(k_1, k_2)$ of equations (5a) and (5b).

13

14

1   **Table 4a:** $UX_3(k_1, k_2) = X(q)\cos[\Delta(k_1) + \Delta(k_2)] + Y(q)\sin[\Delta(k_1) + \Delta(k_2)]$

2

k_2 / k_1	1	2	3	4
1	$X(q)$	$Y(q)$	$-X(q)$	$-Y(q)$
2	$Y(q)$	$-X(q)$	$-Y(q)$	$X(q)$
3	$-X(q)$	$-Y(q)$	$X(q)$	$Y(q)$
4	$-Y(q)$	$X(q)$	$Y(q)$	$-X(q)$

3

4

5   **Table 4b:** $UY_3(k_1, k_2) = Y(q)\cos[\Delta(k_1) + \Delta(k_2)] - X(q)\sin[\Delta(k_1) + \Delta(k_2)]$

k_2 / k_1	1	2	3	4
1	$Y(q)$	$-X(q)$	$-Y(q)$	$X(q)$
2	$-X(q)$	$-Y(q)$	$X(q)$	$Y(q)$
3	$-Y(q)$	$X(q)$	$Y(q)$	$-X(q)$
4	$X(q)$	$Y(q)$	$-X(q)$	$-Y(q)$

6

7   It should be noted that each row in Tables 2-4 is a cyclic shift of the previous row. This

8   fact gives additional opportunity for simplification of the computation procedure as it is

9   necessary to store only four numbers for the computation of the final sixteen numbers.

10

11   Finally, using the results from Tables 4a and 4b, Tables 5a and 5b contain the 3-

12   symbol quadrature components VX_3 and VY_3, calculated according to equations (6a) and

13   (6b).

14

1   **Table 5a:** $VX_3 (k_1, k_2) = VX_2 (k_1) + UX_3(k_1, k_2)$

k_2 k_1	1	2	3	4
1	$VX_2(1)+X(q)$	$VX_2(1)+Y(q)$	$VX_2(1)-X(q)$	$VX_2(1)-Y(q)$
2	$VX_2(2)+Y(q)$	$VX_2(2)-X(q)$	$VX_2(2)-Y(q)$	$VX_2(2)+X(q)$
3	$VX_2(3)-X(q)$	$VX_2(3)-Y(q)$	$VX_2(3)+X(q)$	$VX_2(3)+Y(q)$
4	$VX_2(4)-Y(q)$	$VX_2(4)+X(q)$	$VX_2(4)+Y(q)$	$VX_2(4)-X(q)$

2

3

4   **Table 5b:** $VY_3(k_1, k_2) = VY_2(k_1) + UY_3(k_1, k_2)$

k_2 k_1	1	2	3	4
1	$VY_2(1)+Y(q)$	$VY_2(1)-X(q)$	$VY_2(1)-Y(q)$	$VY_2(1)+X(q)$
2	$VY_2(2)-X(q)$	$VY_2(2)-Y(q)$	$VY_2(2)+X(q)$	$VY_2(2)+Y(q)$
3	$VY_2(3)-Y(q)$	$VY_2(2)+X(q)$	$VY_2(2)+Y(q)$	$VY_2(2)-X(q)$
4	$VY_2(4)+X(q)$	$VY_2(4)+Y(q)$	$VY_2(4)-X(q)$	$VY_2(4)-Y(q)$

5

6   The components of Tables 5a and 5b provide the basis for making a final decision

7   according to algorithm (6c). In the case of DQPSK there are four possible phase

8   differences, (i.e., the differences set forth in (7)), and for purpose of simplification we can

9   designate the corresponding decisions with numbers 1, 2, 3 and 4. These numbers for the

10   third symbol of 3-symbol DQPSK processing are shown in Table 6. The decision

11   corresponds to the location of the maximum according to equation (6c). This means that

12   if, for example, the maximum of $[VX_3(k_1, k_2)]^2 + [VY_3(k_1, k_2)]^2$ is achieved at $k_1=2$ and

13    $k_2=3$, then the decision is 3. So, for a one-symbol decision it is sufficient to determine a

14   column number in Table 6, in which the maximum of equation (6c) takes place.

1   **Table 6**. Decisions for the third symbol of 3-symbol processing of DQPSK.

k_1 \ k_2	1	2	3	4
1	1	2	3	4
2	1	2	3	4
3	1	2	3	4
4	1	2	3	4

2

3   Joint decisions for the second and third symbols of the 3-symbol DQPSK

4   processing are shown in Table 7. As in the previous case, a decision corresponds to

5   location of the maximum according to equation (6c). Thus, for example, if the maximum

6   of $[VX_3(k_1, k_2)]^2 + [VY_3(k_1, k_2)]^2$ is achieved at $k_1=3$ and $k_2=4$, then the decision is 3 for

7   the second symbol, and the decision is 4 for the third symbol. Generally, all sixteen

8   components $[VX_3(k_1, k_2)]^2 + [VY_3(k_1, k_2)]^2$ should be compared to find the maximum.

9

10   **Table 7**. Joint decisions for the second and third symbols of 3-symbol

11   processing of DQPSK.

12

k_1 \ k_2	1	2	3	4
1	1,1	1,2	1,3	1,4
2	2,1	2,2	2,3	2,4
3	3,1	3,2	3,3	3,4
4	4,1	4,2	4,3	4,4

13

1   Turning back to the schematic diagram in Fig. 3, it should be appreciated that in

2   the case of DQPSK, the intersymbol processor IP_1 provides the computations of Table 1,

3   and the intersymbol processor IP_2 provides the computations of Tables 5.

4

5   Fig. 4 shows additional details of the intersymbol processor IP_2 and memories R_1

6   and R_2 for the 3-symbol noncoherent demodulator of DQPSK signals. The intersymbol

7   processor IP_2, shown within dotted lines, includes a four-cell circular shift register (CSR)

8   and two adders A_1 and A_2. Memories R_1 and R_2 are four-cell shift registers. As seen in

9   Fig. 4, there are four signals received at the input to the memories R_1 and R_2 and to

10   intersymbol processor IP_2 including: the current quadrature components $X(q)$ and $Y(q)$ of

11   the received signal, and numbers VX_2 and VY_2 from the output of the previous

12   intersymbol processor IP_1. Numbers $X(q)$ and $Y(q)$ are saved in the four cells of the CSF

13   as positive and negative values as indicated in Fig. 4 and as required by Tables 4a and 4b.

14   In addition, four numbers VX_2 are saved in register R_1 and four numbers of VY_2 are

15   saved in register R_2, all of which are output from intersymbol processor IP_1.

16

17   The calculation procedure in the intersymbol processor IP_2 consists of four

18   cycles, each cycle having four subcycles. During the four subcycles of a first cycle, the

19   first components of VX_2 and VY_2 are sequentially summed in the adders A_1 and A_2 with

20   all four elements of the CSR (with the numbers in the CSR circularly shifting or rotating

21   between each subcycle). The first cycle generates the first rows of Tables 5a and 5b. As

22   seen in Fig. 4, the addition of VX_2 and VY_2 with numbers in the CSR is done in parallel,

23   with VX_2 being added to the number in the last cell of the CSR, and VY_2 being added to

24   the next-to-last cell of the CSR. After the first cycle, the numbers in the shift registers R_1

25   and R_2 are shifted such that the next component of VX_2 and VY_2 may be sequentially

26   summed in the adders A_1 and A_2 with all four elements of the CSR to provide the next

1 line of Tables 5a and 5b. The process continues until all four components of VX_2 and

2 VY_2 stored in registers R_1 and R_2 are added with all four elements of the CSR according

3 to Tables 5a and 5b. After each cycle, numbers in shift registers R_1 and R_2 are shifted,

4 setting free space for the next symbol data.

5

6 The results of the interprocessor IP_2 is to provide sixteen sets of values (VX_3, VY_3)

7 for the decision block. Fig. 5 shows a schematic diagram of the decision block. Two

8 numbers at a time from the output of the intersymbol processor IP_2 are fed to squarers or

9 multipliers M_1 and M_2, the outputs of which are then combined in an adder A_3 in order to

10 implement relationship (6c). The resulting sequence of numbers W_i from the output of

11 the adder A_3 is fed to a logic element 30 which compares each incoming number to a

12 variable V which is initialized as V=0. If at comparator 32, the current number $W_i > V$,

13 then V is replaced by W_i in a memory 34 of variable V. In total, sixteen numbers W_i are

14 compared in the case of the 3-symbol processing of DQPSK signals to find the maximum

15 value. If a decision for only the third symbol is desired, the index "i" of number W_i at the

16 output of the comparator 32 can be transformed at 36 into j=i mod4 such that each new

17 number "j" replaces the previous one in a memory 38 of variable j. According to Table 6,

18 the final value of variable "j" is the desired decision for the third symbol. However, for a

19 joint two-symbol decision (i.e., decisions for the second and third symbols), logic unit 30

20 should operate according to Table 7, with index "i" defining both k_1 and k_2 in order to

21 provide a decision for a single element of Table 7 with maximum value W_i. Thus, for

22 example, if W_7 proved to be a maximum, $k_1=2$ and $k_2=3$, the decision would be 2 for the

23 second symbol and 3 for the third symbol. Similarly, if W_9 proved to be a maximum,

24 $k_1=3$ and $k_2=1$, the decision would be 3 for the second symbol and 1 for the third symbol.

25

1   Given the above, it will be appreciated by those skilled in the art that the

2 invention can be generalized to provide a symbol-by-symbol decision making algorithm

3 for M-ary DPSK at an N-symbol processing interval. In particular, consider DPSK

4 modulation with an arbitrary set of phase differences. The algorithm of N-symbol

5 processing of the q-th received symbol X(q),Y(q) is carried out with (N-1) recurrent steps

6 (iterations).

7

8   Let $VX_{i+1}(k_1, k_2, ..., k_i)$ and $VY_{i+1}(k_1, k_2, ..., k_i)$ be quadrature components at the

9 i-th step, and $UX_{i+1}(k_1, k_2, ..., k_i)$ and $UY_{i+1}(k_1, k_2, ..., k_i)$ be transforms of the received

10 symbol at the i-th step, where i=1, 2,..., N-1. These components and transforms are

11 functions of integer variables $k_1, k_2, ..., k_i$, running from 1 to M. Then, transforms

12 $UX_{i+1}(k_1, k_2, ..., k_i)$ and $UY_{i+1}(k_1, k_2, ..., k_i)$ of the received symbol at the i-th step can be

13 calculated according to the following which is similar to equations (5a) and (5b):

14

15 $UX_{i+1}(k_1, k_2, ..., k_i) = X(q-N+i+1)\cos[\Delta(k_1)+...+ \Delta(k_i)] + Y(q-N+i+1)\sin[\Delta(k_1)+...+ \Delta(k_i)]$ (8a)

16 $UY_{i+1}(k_1, k_2, ..., k_i) = Y(q-N+i+1)\cos[\Delta(k_1)+...+ \Delta(k_i)] - X(q-N+i+1)\sin[\Delta(k_1)+...+ \Delta(k_i)]$, (8b)

17 where q is a symbol number which is currently under the decision making procedure.

18

19   Now the i-th step (iteration) of the desired recurrent algorithm can be represented

20 with the following simple formula:

21

22      $VX_{i+1}(k_1, k_2, ..., k_i) = VX_i(k_1, k_2, ..., k_{i-1}) + UX_{i+1}(k_1, k_2, ..., k_i),$ (9a)

23      $VY_{i+1}(k_1, k_2, ..., k_i) = VY_i(k_1, k_2, ..., k_{i-1}) + UY_{i+1}(k_1, k_2, ..., k_i),$ (9b)

24 where i=1,2,...,N-1, and where $k_i = 1,2,...,M$, and where $VX_1=X(q-N+1),$

1    $VY_1 = Y(q-N+1)$ are quadrature components of the first received symbol in the sequence

2   of N processing symbols.

3

4   A final N-symbol decision regarding the q-th transmitted symbol corresponds to

5   the maximum of a calculated vector at the $i=(N-1)$-th step of the recurrent procedure, i.e.

6

7   Max $\{[VX_N(k_1, k_2, ..., k_{N-1})]^2 + [VY_N(k_1, k_2, ..., k_{N-1})]^2\}$,   (9c)

8

9   where the maximum is determined through all "k".

10

11   It should be noted that decision algorithm (9c), which is similar to algorithm (6c)

12   for 3-symbol processing, may be used for both a symbol-by-symbol decision and a joint

13   decision on (N-1) symbols simultaneously. In the case of a symbol-by-symbol decision,

14   maximization in (9c) is provided through indexes k_{N-1}, corresponding to phase differences

15   between the (N-1)-th and N-th symbols. In the case of the joint symbol decisions,

16   maximization in (8c) is provided through the whole set of indexes $k_1, k_2, ..., k_{N-1}$,

17   corresponding to phase differences between all N symbols participating in N-symbol

18   processing procedure.

19

20   To reiterate, according to the invention, an N-symbol noncoherent algorithm for

21   DMPSK signals can be described as follows:

22

23   a) N consecutive symbols with indexes q, (q-1), ..., (q-N+1) participate in making a

24   decision about the current q-th symbol, and the corresponding quadrature

25   components of the received signals X(q),Y(q); X(q-1),Y(q-1); ...;

26   X(q-N+1),Y(q-N+1) are saved;

1   b) A set of quadrature components $X(q), Y(q)$; $X(q-1), Y(q-1)$; ...; $X(q-N+1)$,

2        $Y(q-N+1)$ are subjected to a $(N-1)$-step transformation;

3   c) The i-th step, where $i=1,2,...,N-1$, includes

4   (1) Calculation of multi-dimensional transforms $UX_{i+1}(k_1, k_2,..., k_i)$ and

5            $UY_{i+1}(k_1, k_2, ..., k_i)$ of the current received components $X(q-N+i+1)$ and

6            $Y(q-N+i+1)$ according to equations (8a) and (8b); and

7   (2) Calculation of mult-dimensional components $VX_{i+1}(k_1, k_2,..., k_i)$ and

8            $VY_{i+1}(k_1, k_2,..., k_i)$ according to recurrent formulas (9a) and (9b);

9   d) Final decision relative to the current q-th symbol is the phase difference from

10   the set of differences $\Delta(k_{N-1})$, where $k_{N-1}=1, 2,..., M$, corresponding to the

11   maximum of the length of vectors $[VX_N(k_1, k_2, ..., k_{N-1}), VY_N(k_1, k_2, ..., k_{N-1})]$,

12   according to algorithm (9c);

13

14   Turning now to Fig. 6, a schematic diagram is provided of the N-symbol

15   noncoherent demodulator of DMPSK signals which implements equations (9a) and (9b).

16   The apparatus of Fig. 4 includes $(N-1)$ Intersymbol Processors $IP_1...IP_{N-1}$; $(N-2)$ pairs of

17   memory blocks $VX_2, VY_2...VX_{N-1}, VY_{N-1}$, a Decision block, and two memories for signal

18   quadrature components X and Y, which are depicted as Shift Registers SR_x and SR_y.

19

20   The apparatus of Fig. 6 operates as follows. Quadrature components of the

21   current received symbol $X(q)$ and $Y(q)$ are directly fed to the IP_{N-1}. In addition,

22   component $X(q)$ is inserted into the first (right-hand) cell of SR_x, shifting all register

23   elements by one cell from right to left, and component $Y(q)$ is inserted into the first

24   (right-hand) cell of SR_y, shifting all register elements by one cell from right to left. As

25   seen in Fig. 6, storage locations of both memory shift registers SR_x and SR_y are connected

26   to corresponding intersymbol processors IP. Each IP, in turn, receives signals from

1   registers SR_x and SR_y as well as results of computations of the previous IP stored in

2   corresponding memories VX_j and VY_j. All intersymbol processors provide computations

3   according to equations (8) and (9a) and (9b), but the number of operations carried out by

4   each IP is different. For example, IP_1 calculates M complex numbers, and IP_{N-1} calculates

5   M^{N-1} complex numbers per symbol. Thus, for 4-symbol processing of DQPSK, the first

6   IP will calculate four numbers, while the last IP will calculate sixty-four numbers. As

7   shown above, in the proposed algorithms all computations are simple summing

8   operations of two numbers (see Tables 1-5). A final decision is provided in the Decision

9   block according to algorithm (9c).

10

11   It should be appreciated by those skilled in the art that Fig. 6 illustrates only the

12   functions of the proposed multisymbol noncoherent demodulator and not necessarily its

13   most desirable implementation. Indeed, there are numerous ways to implement the

14   proposed recurrent algorithm of equations (9a) and (9b) and the sequence of operations

15   provided by apparatus in Fig. 4. For example, all operations provided by the individual

16   intersymbol processors of Fig. 6 can be combined in a single high-speed intersymbol

17   processor. Likewise, all memory and shift register storage can be provided in a single

18   block of memory.

19

20   Fig. 7 provides a high level block diagram of an alternative implementation of the

21   multisymbol demodulator of the invention. The apparatus of Fig. 7 includes a single

22   intersymbol processor IP (which may be implemented in a DSP, discrete components, or

23   in software of a general-purpose processor), X-memory and Y-memory blocks (which

24   may be part of a single memory such as a RAM, or separate memory elements), and a

25   Decision block. The X-memory stores components X(q-N+2), X(q-N+3), ..., X(q-1) of

26   the received signal as well as intermediate results of intersymbol processing VX_j

1   (j=2,3,...,N-1). Similarly, the Y-memory stores components Y(q-N+2), Y(q-N+3), ...,

2   Y(q-1) of the received signal as well as intermediate results of intersymbol processing VY_j

3   (j=2,3,...,N-1). The Intersymbol Processor (IP) calculates all intermediate components

4   VX_j and VY_j as well as final values VX_N and VY_N according to equations (8) and (9a) and

5   (9b).

6

7   The DBPSK and DQPSK modulation techniques described above were simulated

8   by means of stochastic simulation programs which were programmed to compare perfect

9   coherent processing with noncoherent processing having different processing intervals

10 according to the invention. Simulation results for DBPSK and DQPSK modulation

11 techniques are shown in Fig. 8 and Fig. 9. More particularly, Fig. 8 shows the bit error

12 rate (BER) as a function of signal-to-noise ratio (SNR) in dB for DBPSK modulation.

13 The lowest (solid) curve corresponds to perfect coherent processing of the DBPSK signal,

14 while the remaining curves (from top to bottom) correspond to noncoherent processing

15 according to the invention with 2, 3, 4, and 5-symbol intervals.

16

17   At least two conclusions can be deduced from the simulation results. First, in the

18 case of DBPSK there does not appear to be any reason to increase the processing interval

19 beyond five symbols, because with 5-symbol interval the system already approximates

20 minimum possible BER, which is approximately twice the BER for the perfect coherent

21 processing of BPSK. This conclusion is illustrated in Table 8, which shows BER vs. SNR

22 for BPSK with perfect coherent processing, DBPSK with perfect coherent processing, and

23 DBPSK with 5-symbol noncoherent processing.

24

25

26

1   **Table 8** BER vs. SNR for BPSK and DBPSK

2

SNR dB	BER BPSK (Perfect Coherent)	BER DBPSK (5-symbol noncoherent)	BER DBPSK (Perfect Coherent)
7.5	4.0 E-4	1.0 E-3	8.0 E-4
8.0	2.0 E-4	4.5 E-4	4.0 E-4
8.5	8.5 E-5	1.8 E-4	1.7 E-4

3

4   A second conclusion is that in the case of DBPSK the most considerable

5   improvement takes place at the transition from 2-symbol processing to 3-symbol

6   processing; it being evident from Fig. 8 that the dashed line of 2-symbol DBPSK is

7   further away from the dashed line of 3-symbol DBPSK than the dashed line of 3-symbol

8   DBPSK is from the dotted line of 4-symbol DBPSK. For example, at a BER of $4x10^{-4}$,

9   going from 2-symbol DBPSK to 3-symbol DBPSK yields a gain of slightly over .3dB,

10   whereas increasing from 3-symbol DBPSK even to 5-symbol DBPSK will yield a gain of

11   only about another .1dB. So, from a practical point of view, it may be desirable to use 3-

12   symbol pilotless noncoherent processing for best performance gain with limited signal

13   processing costs.

14

15   Fig. 9 shows the bit error rate (BER) as a function of signal-to-noise ratio (SNR)

16   in dB for DQPSK modulation. The lowest solid curve corresponds to perfect coherent

17   processing of the DQPSK signal, with the remaining curves (from top to bottom)

18   corresponding to noncoherent DQPSK processing with 2, 3, 4, and 5-symbol intervals.

19   As was the case for DBPSK, the most considerable improvement in DQPSK takes place

20   when going from 2-symbol processing to 3-symbol processing. Further improvement

21   decreases as the number of processing symbols increases. However, practically, 4-

1   symbol processing is a good option for DQPSK modulation, because the gain is still

2   rather significant between 3-symbol and 4-symbol processing. For example, at a BER of

3   7×10^{-3}, going from 2-symbol processing (the top dashed line) to 3-symbol processing (the

4   next dashed line) yields a gain of almost .5dB. Going from 3-symbol processing (the

5   second dashed line) to 4-symbol processing (the dotted line) yields a similar, albeit

6   slightly smaller gain of over .4dB. However, going from 4-symbol processing to 5-

7   symbol processing yields only approximately .1dB. Thus, 4-symbol DQPSK would

8   appear to give the best performance gain relative to the additional complexity in

9   processing.

10

11   There have been described and illustrated herein several embodiments of

12   methods, apparatus, and systems for implementing non-coherent processing of pilotless

13   telecommunication signals. While particular embodiments of the invention have been

14   described, it is not intended that the invention be limited thereto, as it is intended that the

15   invention be as broad in scope as the art will allow and that the specification be read

16   likewise. Thus, while particular hardware and logic elements have been disclosed for

17   implementing the invention, it will be appreciated that the invention could be

18   implemented using different hardware and logic elements as well. In addition, the

19   invention can be implemented with software and firmware as well. It will therefore be

20   appreciated by those skilled in the art that yet other modifications could be made to the

21   provided invention without deviating from its spirit and scope as claimed.

22